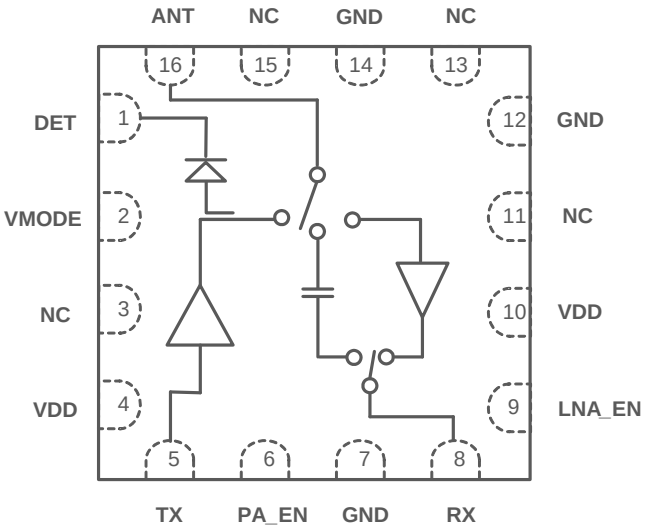
2.4GHZ CMOS WLAN / BT DUAL-MODE RFEIC WITH PA, LNA & SP3T



DESCRIPTION

RFX8425 is a pure CMOS-based, single-chip/single-die RFeIC (RF Front-end Integrated Circuit) that incorporates all key RF functionality needed for implementing high-performance RF front-end for WLAN IEEE 802.11b/g/n and OFDM/256QAM operation in the 2.4GHz band. The RFX8425 architecture integrates a high-efficiency high-linearity power amplifier (PA) with harmonic filter, a directional coupler based power detector, a low noise amplifier (LNA), an SP3T switch for Bluetooth antenna sharing, and an additional SPDT switch for selection between LNA and Bypass in Receive mode. All the impedance matching components and DC-block capacitors are also integrated to minimize the PCB footprint for system implementation.

RFX8425 is assembled in an ultra-compact, low-profile 2.3x2.3x0.45mm 16L QFN package. It has simple and low-voltage CMOS control logic, and requires minimal external components. Designed to work in the 3.0-3.6V voltage range, the RFX8425 is ideal RF front-end solution for implementing 2.4GHz WLAN/BT in PC clients, tablets, and many other mobile platforms including smartphones that have a PMIC available to provide the required supply voltage for the RF front-end.

FEATURES

- Combines 802.11b/g/n/ac and Bluetooth applications
- High linearity PA for 802.11 b/g/n/ac WLAN
- Low Noise Figure WLAN Receive LNA with Bypass for Near Range Operation
- Built in directional coupler based output power detector
- ESD Protection Circuitry on All Ports
- DC decoupled RF Ports and VDD / RF Isolation
- 2.3x2.3x0.45mm Small Outline 16L QFN Package with Exposed Ground Pad

APPLICATIONS

- Smartphones, Feature Phones and MIDs with WLAN/Bluetooth
- WLAN/Bluetooth Platforms Requiring Shared Antenna
- Laptop / Netbook / Smartbook with Embedded WiFi & Bluetooth
- Portable Platforms with Integrated 802.11b/g/n and Bluetooth
- RoHS and REACH Compliant

Skyworks Solutions, Inc. • Phone [781] 376-3000 • Fax [781] 376-3100 • sales@skyworksinc.com • www.skyworksinc.com

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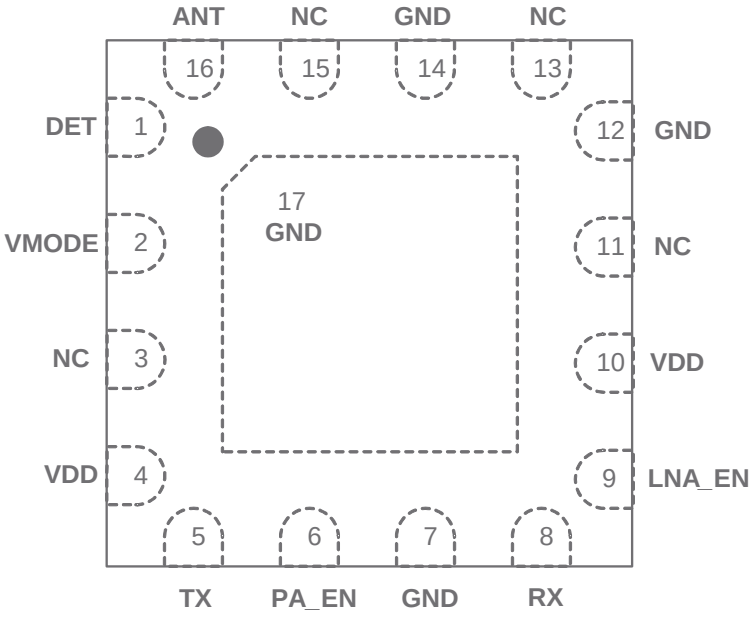
Package Pin out and Pin Description



(Top "See-Through" View)

Pin Number	Pin Name	Description
1	DET	PA Power Detector Output Voltage
2	VMODE	CMOS Logic Control Used for PA Mode Control in Rome Platform; Unused for Rhino Platform.
4, 10	VDD	DC Voltage Supply
5	TX	WLAN TX Signal Port from the Transceiver; DC Shorted to GND
6	PA_EN	CMOS Logic Control to Enable WLAN Transmit
8	RX	WLAN RX Signal Port to the Transceiver/BT Port; DC Shorted to GND
9	LNA_EN	CMOS Logic Control to Enable LNA
3, 11, 13, 15	NC	Not Connected Internally. Can be Grounded or Left Open
7, 12, 14, 17	GND	Ground – Must be Connected to Ground in the Application Circuit
16	ANT	RF Signal Port to/from the Antenna: DC Shorted to GND

ABSOLUTE MAXIMUM RATINGS

Parameters	Unit	Min.	Max.	Conditions
DC VDD Voltage Supply	V	-0.3	4	All VDD Pins
DC Control Pin Voltage	V	-0.3	3.6	All Control Pins
DC current consumption	mA		350	PA_EN = High
TX RF Input Power	dBm		+10	
ANT RF Input Power	dBm		+20	Bypass Mode
Junction Temperature	°C		150	
Operating Ambient Temperature	°C	-20	+85	
Storage Ambient Temperature	°C	-40	+150	Appropriate care required according to JEDEC Standards

Note: Sustained operation at or above the Absolute Maximum Ratings for any single or combinations of the above parameters may result in permanent damage to the device and is not recommended.

All Maximum RF Input Power Ratings assume 50-Ohm terminal impedance.

NOMINAL OPERATING CONDITIONS

Parameters	Unit	Min	Typ	Max	Conditions
VDD Voltage Supply *(Note 1)*	V	3.0	3.3	3.6	All VDD Pins
RF Port Impedance	Ω		50		Single-Ended
Control Voltage "High" *(Note 2)*	V	1.2		3.6	
Control Voltage "Low"	V	0		0.4	
Control Pin Current	µA		1		
Shutdown Current	µA		6		PA_EN = Low, LNA_EN = Low
PA Turn On/Off Time	µs			0.4	
LNA Turn On/Off Time	µs			0.4	
θ_{jc} *(Note 3)*	°C/W		29		
θ_{ja}	°C/W		45		

Note 1: For normal operation of the RFX8425, VDD must be continuously applied to all VDD supply pins.
Note 2: If control voltage can exceed 2.0V, a 1KΩ – 10KΩ series resistor is recommended for the application circuit on each control line.
Note 3: Thermal measurements were performed on an RFaxis test EVB under typical use conditions. Please contact RFaxis for details regarding the test conditions and the configuration of the thermal vias on the EVB. Refer to "PCB Land Pattern" for recommended thermal vias.

TRANSMIT PATH CHARACTERISTICS (VDD=3.3V, T_a=+25° C)

Parameters	Unit	Min	Typ	Max	Conditions
Operating Frequency	GHz	2.4		2.5	
Linear Output Power for 802.11ac	dBm		+18		Dynamic EVM < -35dB for MCS9/VHT40
Linear Output Power for 802.11n	dBm		+18.5		Dynamic EVM < -32dB for MCS7/HT20
Linear Output Power for 802.11g	dBm		19		Dynamic EVM < -32dB for 64QAM/54Mbps
Linear Output Power for 802.11b	dBm		22		For 802.11b 1Mbps CCK Mask Compliance with 1.5dB Margin
Total Supply Current for 802.11ac	mA		140		For Pout = +18dBm, MCS9/VHT40
TX Small Signal Gain	dB		26		
Second Harmonics	dBm/MHz		-8		P_{OUT} = +22dBm, 11b 1Mbps CCK
Third Harmonics	dBm/MHz		-27		P_{OUT} = +22dBm, 11b 1Mbps CCK
Power Detector Voltage	mV		250 - 1000		Measured with 10kΩ load, P_{OUT} = +5 to +20dBm
Input Return Loss	dB		-12		
Output Return	dB		-6		

RECEIVE PATH CHARACTERISTICS (VDD=3.3V, T_a=+25° C)

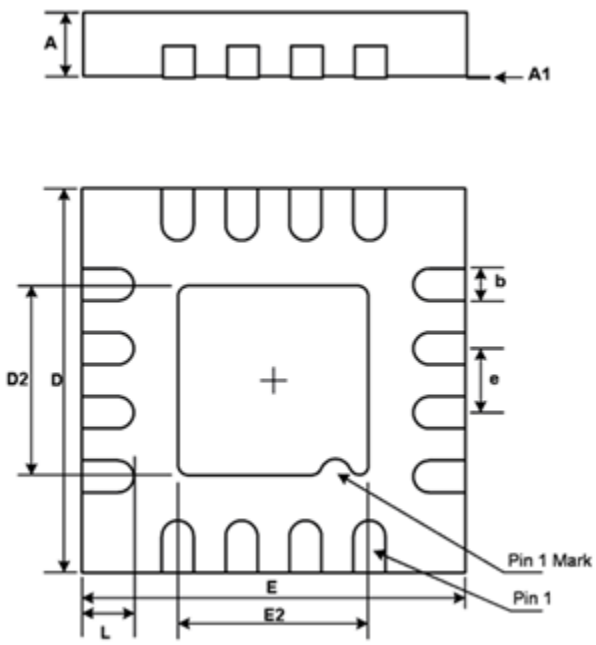
Parameters	Min	Typ	Max	Unit	Conditions
Operating Frequency	2.4		2.5	GHz	
Small-Signal Gain (High Gain Mode)		16		dB	
Noise Figure		2.6		dB	
LNA Quiescent Current		12		mA	
IIP3		+3.0		dBm	
Insertion Loss (Bypass Mode)		1.5		dB	

TRUTH TABLE

PA_EN	LNA_EN	VMODE	Mode of Operation
0	0	X	Bypass / Sleep Mode
1	0	0	High Linearity Transmit Mode
0	1	X	Receive Mode with LNA ON
1	0	1	Power Save Transmit Mode
1	1	X	Power Save Transmit Mode

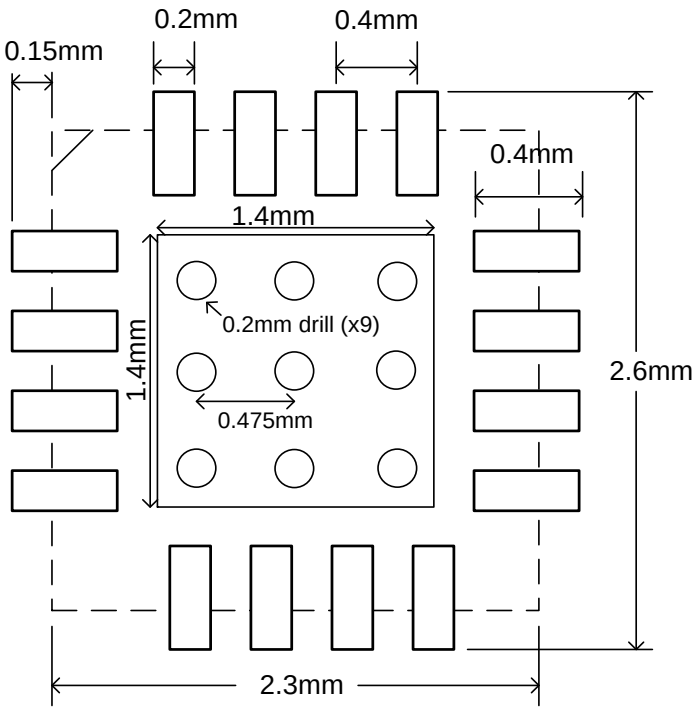
Note: "1" denotes high state (> 1.2V), "0" denotes Low state (< 0.4V), "X" denotes either state (don't care)
1KΩ – 10KΩ series resistor may be required for each control line

PACKAGE DIMENSIONS



Dimensional Ref.			
REF.	Min.	Nom.	Max.
A	0.400	0.450	0.500
A1	0.000	-	0.0
D		2.300 BSC	
E		2.300 BSC	
D2	1.350	1.400	1.450
E2	1.350	1.400	1.450
b	0.150	0.200	0.250
e		0.400 BSC	
L	0.200	0.250	0.300

PCB LAND PATTERN
(With Recommended Thermal Vias)



PACKAGE MARKING